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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,212	11/12/2003	Michael E. Connell	5083.1US (01-0428.01/US)	6326

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EXAMINER	
ECKERT II, GEORGE C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,212 ✓	CONNELL ET AL.	
	Examiner	Art Unit	
	George C. Eckert II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/12/03, 3/11/04, 6/4/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 2, 4, 7, 8, 13, 14, 16, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by US 3,861,969 to Ono et al. Ono et al. teach in figure 4, a die comprising:

a semiconductor substrate 41 having a front and back side, the substrate having a low ration of height to width;

an integrated circuit 44 on a portion of the front side;

a passivation layer 42 covering a portion of the IC which passivation layer inherently causes a stress; and

a stress balancing layer 46 covering at least a portion of the back side.

Ono et al. also teach that the stress-balancing layer comprises a single component layer of Au-Ge, Sn or Au-Sn which material may be marked with a laser.

2. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 59-132153 to Yamauchi. Yamauchi teaches in figure 3 a semiconductor die comprising:

a semiconductor substrate 2 having front and back sides;

integrated circuits 5 and 6 formed on a portion of the front side;

passivation layers 9 and 10 covering a portion of the integrated circuits; and

a stress balancing layer 17 covering at least a portion of the back side.

Yamauchi also teaches that the balancing layer is a single component layer and that the device further includes an adhesive 16 attaches to the stress balancing layer. That the adhesive and stress balancing layer may be marked by a laser is considered an inherent function of those layers.

3. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,728,624 to Linn et al. Linn et al. teach in figure 3d a semiconductor die comprising:

a semiconductor substrate 302 having a front and back side;

an integrated circuit on a portion of the front side (col. 3, lines 50-53);

a passivation layer 326 covering a portion of the integrated circuit;

a stress-balancing layer 315, 316 covering at least a portion of the back side.

Linn et al. also teach that the stress balancing layer is comprised of an homogenous mixture of a strong material in a matrix material (col. 3, lines 7-10) and that the SBL is an adhesive (the layers 315/316 are used to adhere wafer 302 to wafer 312). That the adhesive and stress balancing layer may be marked by a laser is considered an inherent function of those layers.

4. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,380,558 to Yamazaki et al. Yamazaki et al. teach, with reference to figures 1A-C, a die comprising:

a substrate 103 having a front side and a back side;

an integrated circuit on a portion of the front side (the TFT formed in the substrate);

a passivation layer 104 covering a portion of the IC; and

a stress balancing layer 102b covering at least a portion of the back side (col. 7, lines 50-55).

Yamazaki et al teach that the SBL is a single component layer and provides adhesion by between itself and the lower substrate 101. Yamazaki et al also teach an adhesive layer 102a attached to SBL 102b. That the adhesive and stress balancing layer may be marked by a laser is considered an inherent function of those layers.

5. Claims 1, 7, 13 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by US 2003/0207095 to Lowack et al. Lowack et al. teach in paragraphs 0002-03 that it is known to form a stress balancing layer (substrate back coating) on the back side of a semiconductor substrate having ICs formed therein and a passivation layer (insulating material) formed on the ICs, the purpose of the back coating "to lessen stress induced substrate flexion" (para. 0003).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 4, 7, 8, 13, 14, 16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art shown in figure 2B in view of US 2003/0017626 to Hilt et al. Applicant's prior art teaches the limitations of a semiconductor substrate 20B having a front and back side, integrated circuit portion on the front side, and a passivation layer on the integrated circuit portion that causes stress. However, applicant's prior art does not teach a stress-balancing layer on the back side.

Hilt et al teach in figure 26 a stress balancing layer 70 formed on the back side of a substrate 22 in which ICs are formed on the front side. Hilt et al. also teach that the SBL is a single layer that may be comprised of a dielectric, metal or semiconductor (para. 0096). Applicant's prior art and Hilt et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of applicant's prior art using the SBL as taught by Hilt et al. The motivation for doing so, as is taught by Hilt et al., is that such an SBL will decrease or control the propagation of dislocations in the semiconductor structure (para. 0096, second sentence). Therefore, it would have been obvious to combine Applicant's prior art and Hilt et al. to obtain the invention of claims 1, 2, 4, 7, 8, 13, 14, 16, 19 and 20.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional art teaches the formation of a stress balancing layer on the back side of a substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (571) 272-1728. The examiner can normally be reached on 8:00 - 5:30, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GEORGE ECKERT
PRIMARY EXAMINER